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High Speed and Low Power Dynamic Latched Comparator for PTL Circuit Applications

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***Abstract*— Comparators are basic building blocks for designing modern mixed signal systems. Speed and resolution are two important factors which are required for high speed applications. This paper presents a design for an on-chip high-speed dynamic latched comparator for high frequency signal digitization. The dynamic latched comparator consists of two cross coupled inverters comprising a total of 9 MOS transistors. The measurement and simulation results show that the dynamic latched comparator design has higher speed, low power dissipation and occupying less active area compared to double tail latched and pre-amplifier based clocked comparators. These comparators are used in PTL circuits, so we compared the application of a PTL circuits by using the above specified three comparator designs. The simulation results show that PTL circuit with dynamic latched comparator has occupied less active area and also having higher speed and lower power dissipation. The comparator schematics and corresponding layouts are implemented using spice and microwind tool.**

***Keywords*— Dynamic Latched Comparator, digitization**

I. INTRODUCTION

The comparator compares the voltages that appear at their inputs and outputs a voltage representing the sign of the net difference between them. Comparators are important elements in modern mixed signal systems. Speed and resolution are two important features which are required for high speed applications such as on-chip high frequency signal testing, data links, sense amplifiers and analog-to-digital converters. On-chip testing of high frequency pseudo random binary sequences (PRBS) requires a high speed comparator at the electrical interface stage [1], [2].

A clocked comparator generally consists of two stages. In that first stage is to interface the input signals. The second (regenerative) stage consists of two cross coupled inverters, where each input is connected to the output of the other. In a CMOS based latch, the regenerative stage and its following stages consume low static power since the power ground path is switched off either by a NMOS or PMOS transistor [10].

In many applications comparator speed, power dissipation and transistor count are more important. If comparator speed is a priority, the regenerative stage could be designed to start its operation from midway between power supply and ground [6], for example, conventional comparator2 [4]. However, the static power consumption is relatively high. If comparator was designed with priority given to power reduction, then transistor count increases thereby reducing the speed, for example double tail latched comparator or conventional comparator1[4].

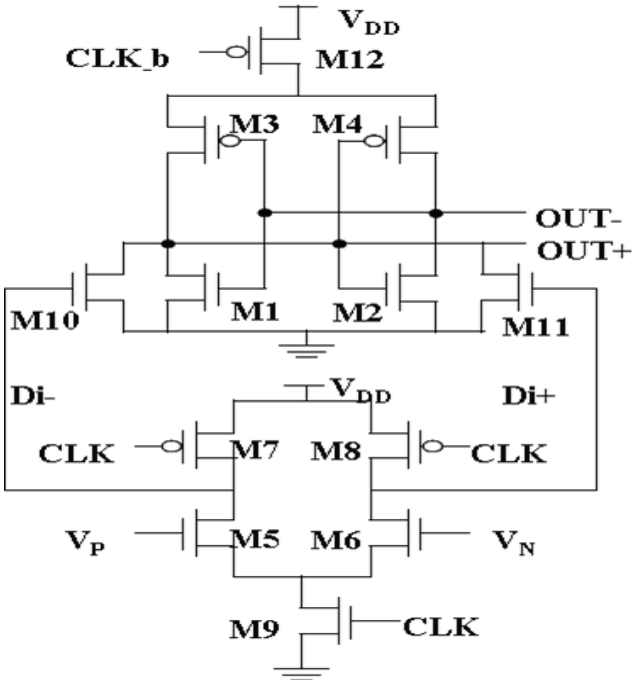
Comparator design largely depends on the target application. However, an input-referred latch offset voltage (hence offset voltage), resulting from the device mismatches such as threshold voltage V_{th}, current factor β (=μ*CoxW/L)* and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of such comparators [8], [9]. In this paper, we present a design of high-speed and low power dissipating clocked comparator for stack circuit applications. The comparator is attractive for the applications where both speed and power consumption are of the highest priority.

The rest of the paper is organized as follows. The speed and power limitations of the two conventional comparators design and areas for improvements are investigated in Section II. An overview of the dynamic latched comparator design [13] is given in Section III. Application of dynamic latched comparator in SAPTL was given in Section IV. The simulation results, comparisons are given in Section V.

II. CONVENTIONAL COMPARATORS

The circuit and schematic diagrams of the comparator presented in [3] are shown in Fig. 1. This comparator is compared with our design because of its speed and suitability for low supply voltage applications. In the rest of the paper it will be referred to as conventional comparator1.It operates in 2 phases 1)Reset phase 2)Regeneration phase .While the clock is low(reset phase), M7 and M8 transistors are ON. M9 transistor is off. As M7 and M8 transistors are ON Di+ and Di- nodes are pre-charged to Vdd. So M10 and M11 become ON and discharge the output nodes OUT+ and OUT- to ground. While the clock is high (regeneration phase), M9 and M12 transistors are in ON condition. M7 and M8 transistors are in OFF state. So Di nodes starts discharging as M9 is ON. The difference between voltages of Di+ and Di- (ΔVDi) are given to M10 and M11 transistors. As Di nodes starts

discharging, M10 and M11 are initially in ON condition and gradually M10 and M11 becomes OFF. Output nodes OUT+ and OUT- starts regenerating when M10 and M11 are unable to ground the outputs. The intermediate stage formed by M10 and Mll passes ΔVDi to the cross-coupled inverters and also provides additional shielding between the input and output, with less kickback noise as a result[8].



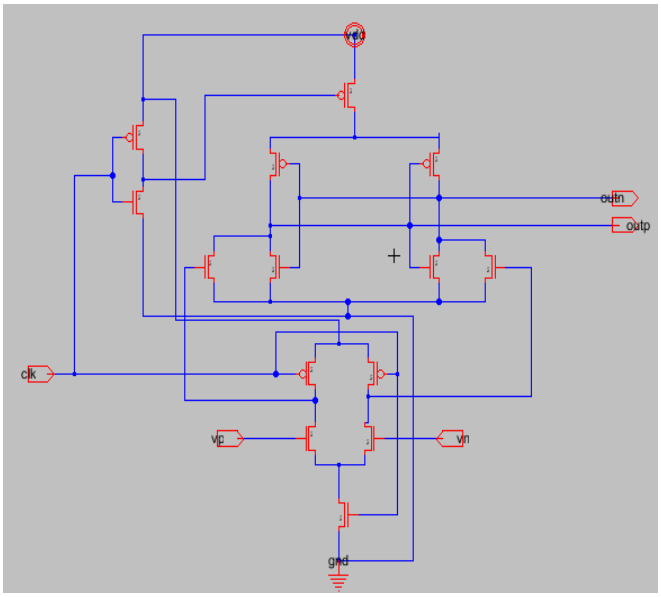


Fig 1 Circuit diagram and Schematic of double tail latched comparator (conventional comparator1)

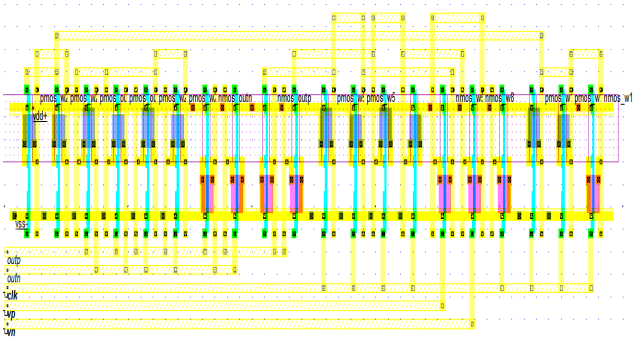
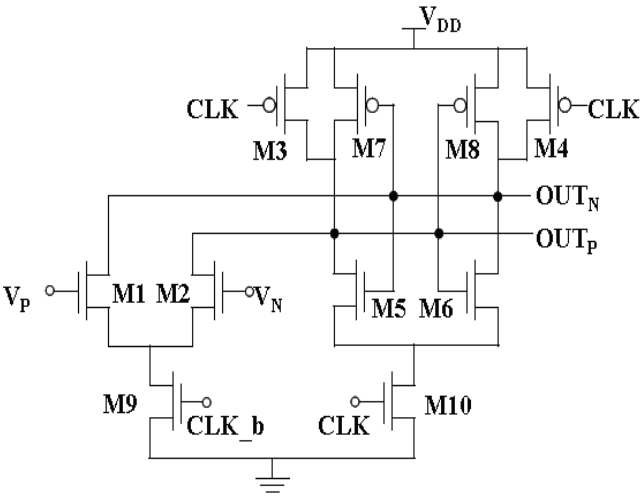


Fig 2 Layout of double tail latched comparator

The conventional comparator2 is composed of two stages as shown in Fig. 3. The first stage is the amplification stage, which consists of the transistors M1–M4 and M9. The second stage is the regenerative stage that is comprised of the transistors M5– M8 and M10. The circuit works in two phases, namely the amplification phase and the regenerative (evaluation) phase. When the clock (CLK) is low (amplification phase), the tail transistor M9 turns ON and M10 turns OFF. When CLK was LOW only amplification stage works here. In addition, the amplification stage is designed to produce its output close to VDD-|Vthp| which can effectively reduce the charging time. In this stage Vp-Vn is amplified and fed to regenerative stage. When the clock (CLK) is high (regeneration phase), M10 turns ON and M9 turns OFF. Only regenerative stage works here.

There is a reduction of the delay time in the conventional comparator2 over the conventional comparator1. Since the conventional comparator2 uses an amplification stage, it consumes static power during the amplification period and hence the energy consumption in the conventional comparator2 becomes higher than the conventional comparator1. There is a reduction of the power dissipation in the conventional comparator1 over the conventional comparator2. In order to avoid these drawbacks in conventional comparators, dynamic latched comparator was introduced in the subsequent section.



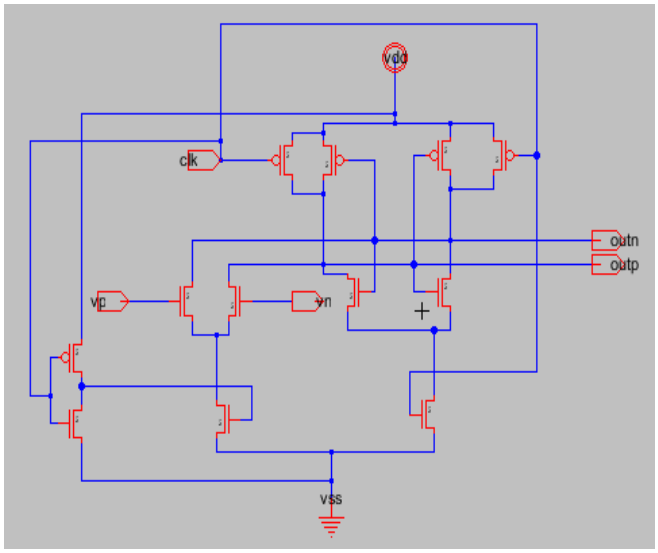


Fig 3 Circuit diagram and Schematic of pre-amplifier based clocked comparator (Conventional comparator2)

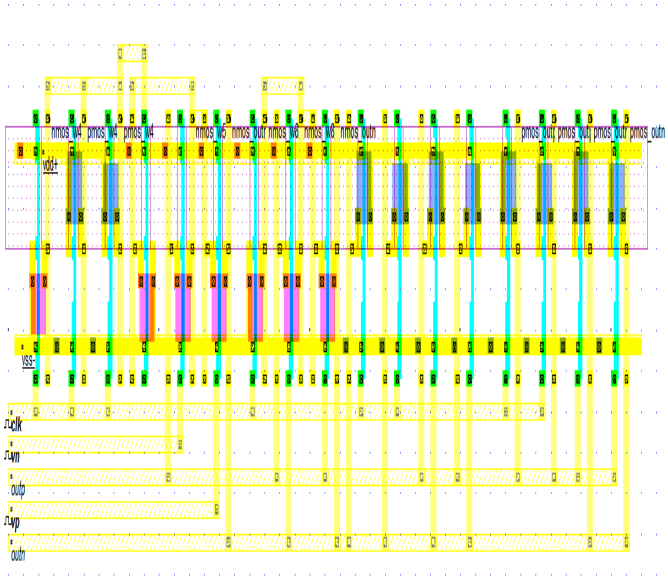


Fig 4 Layout of pre-amplifier based clocked comparator

III. THE DYNAMIC LATCHED COMPARATOR

The dynamic latched comparator is composed of two stages as shown in Fig. 5. The first stage is the interface stage which consists of all the transistors except two cross coupled inverters. The second stage is the regenerative stage that is comprised of the two cross coupled inverters, where each input is connected to the output of the other. It operates in two phases.1) Interface phase and 2) Regeneration phase. It consists of single nmos tail transistor connected to ground. When clock is low tail transistor is off and depending on Vp and Vn output reaches to VDD or gnd. When clock is high tail transistor is on and both the outputs discharges to ground.

There is reduction of both power and delay in dynamic latched comparator circuit over the two conventional comparators. Conventional comparator1 has less power consumption but low speed because of more transistor count and conventional comparator2 has high speed because of less transistor count but power consumption is more because the conventional comparator2 uses an amplification stage, it consumes static power during the amplification period However, since the conventional comparator2 is to work at high frequency, the energy consumption of the conventional comparator2 becomes comparable to the conventional comparator1. Hence the performance of the conventional comparator2 is limited by the static power dissipation in the evaluation or regeneration phase.

The dynamic latched comparator is suitable for both high speed and low power dissipation [12] because of decrease in transistor count which overcomes the problem of two conventional comparators.

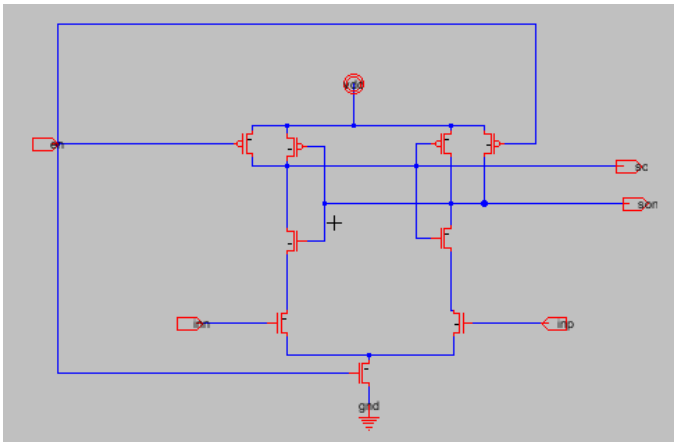


Fig 5 Schematic of Dynamic latched comparator

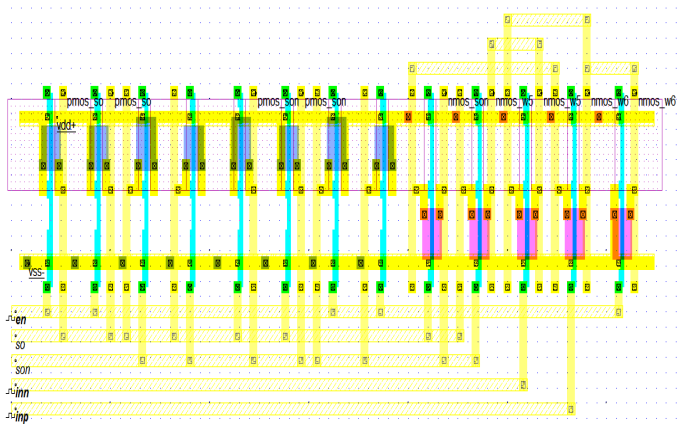


Fig 6 Layout of dynamic latched comparator

TABLE I

Comparison of 3 clocked comparators

Clocked Comparator	Transistor count	Voltage(v)	Power(mw)	Delay(ns)
Double tail Latched comparator	12	1.2	0.006	0.038
Preamplifier based clocked comparator	10	1.2	0.269	0.014
Dynamic latched comparator	9	1.2	0.003	0.011

Since the comparator offset [11] can be reduced by using known techniques [3], the main focus of this paper is the comparator speed and power dissipation. Simulation comparing the delay versus the supply voltage and power dissipation versus the supply voltage of the comparator 1.2V supply has been done. The results show that the dynamic latched comparator outperforms the other 2. Hence the 2 conventional and the dynamic latched comparator will be compared. The layouts are automatically extracted and simulated with a microwind simulator. Fig. 21, 22 shows simulation results of the power dissipation, delay versus supply voltages (V_{dd}) respectively for the dynamic latched comparator and conventional designs. The results show that the dynamic latched comparator circuit has less delay time and less power dissipation than the conventional designs.

As in the dynamic latched comparator circuit design, both the power dissipation and delay will be less [13] as shown in table1. This makes the dynamic latched comparator circuit more attractive for the low power and high speed applications.

IV. .APPLICATION

Both conventional comparators and dynamic latched comparator are used

1) To compare the outputs of stack circuit.
2) Clocked comparator combined with stack circuit acts as OR (or) NOR circuit.

The basic architecture of clocked comparator based PTL is shown in the Figure7. It consists of

1) The pass transistor tree, called the stack. It computes the required logic function.
2) The root driver (inverter) injects signals into the stack and
3) The sense amplifier replaced with clocked comparator is used to compare the stack outputs and also to perform NOR (or) OR operation.

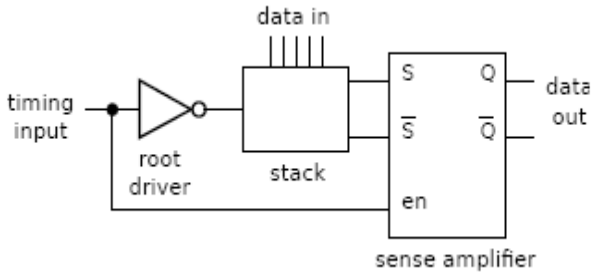


Fig 7 Architecture of clocked comparator based PTL

Stack:

The stack circuit consists of an NMOS pass transistors only. Full-swing inputs are provided to the stack circuit and low-swing pseudo differential outputs are obtained to perform the required logic functions. Fig 8 shows the logical paths of stack circuit that can be connected according to Boolean function using the programmable switches.

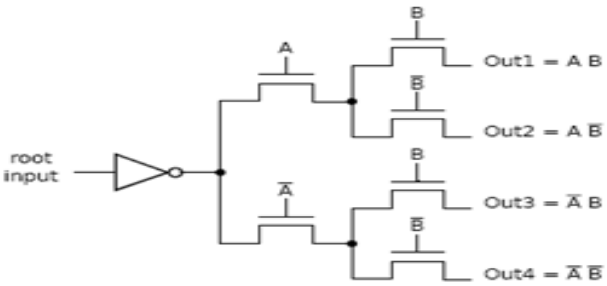


Fig 8 The full stack and driver showing the logic paths

As shown in fig 10 by using the programmable switches, the stack implements a given Boolean expression by connecting the minterm branches of the tree to one output 's' and the maxterm branches to the other output 'sn' such that by drawing karnaugh map we must obtain Boolean expression of OR gate .

Consider the Boolean function of OR (or) NOR gate. In this case for the stack circuit if we provide 'Vin' as '1' then due to inverter, '0' will be provided to stack circuit and stack circuit performs NOR operation. If we provide 'Vin' as '0' then due to inverter, '1' will be provided to stack circuit and stack circuit performs OR operation.

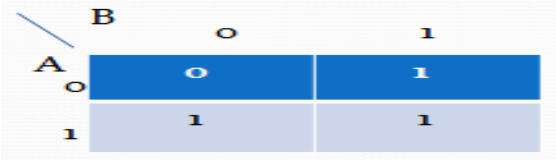


Fig 9. Karnaugh map for OR or NOR gate

Karnaugh map was drawn from fig10 i.e corresponding to connection of programmable switches. According to karnaugh

map the cells that consist of 1's are termed as minterms(01,10,11), and the cells that consist of 0's are termed as maxterms(00). From the karnaugh map we get boolean equation of OR gate i.e A+B.

In stack circuit all the minterms(01,10,11) are connected to 's' output and all the maxterms(00) are connected to output 'sn' as shown in fig 10 to perform OR or NOR operation.

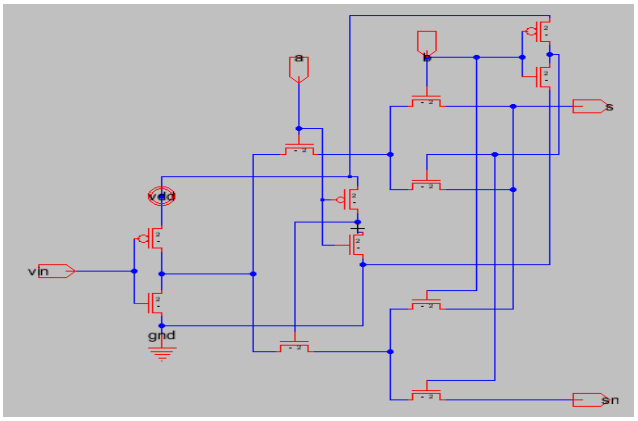


Fig 10. Schematic of the inverted pass transistor tree network configured as a two-input OR/NOR stack.

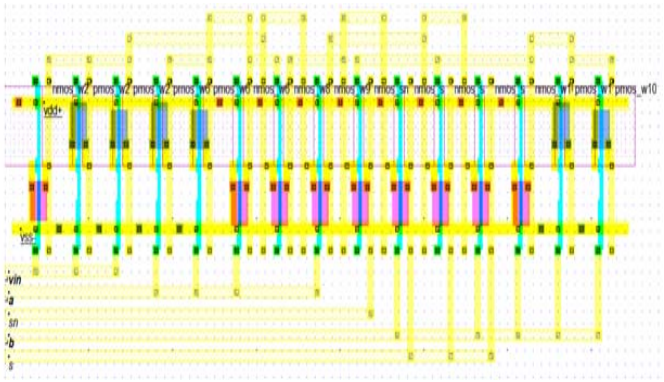


Fig 11. Layout of stack circuit

Driver:

Since the stack has no supply rail connections, a driver, which is a simple inverter, is placed at the root input of the stack, to inject the evaluation current.

Clocked comparator:

In fig7 sense amplifier was used to recover both voltage swing and performance. If we place either of the conventional comparators or dynamic latched comparator in place of sense amplifier, it is useful to perform two operations.

a) To compare the outputs of the stack circuit. As the designed stack circuit performs NOR (or) OR operation, this NOR (or) OR outputs are compared by the clocked comparator.

b) Combination of both Clocked comparator and stack can also be used as NOR (or) OR circuit. I.e. the output of clocked comparator based PTL (stack) is same as stack circuit (NOR (or) OR circuit).

As shown in Fig 12, when 'en' (Vin in case of stack circuit) for the comparator was '1', clocked comparator based PTL acts as NOR circuit. When 'en' (Vin in case of stack circuit) was '0' clocked comparator based PTL acts as OR circuit

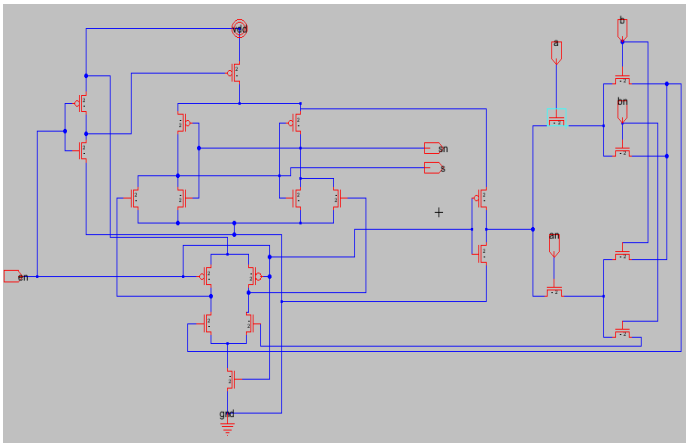


Fig 12. Schematic of Double tail latched comparator based PTL

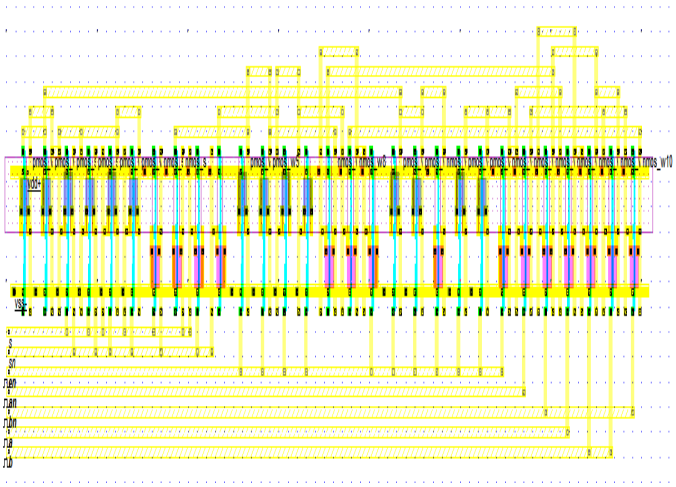


Fig 13 Layout of double tail latched comparator based PTL

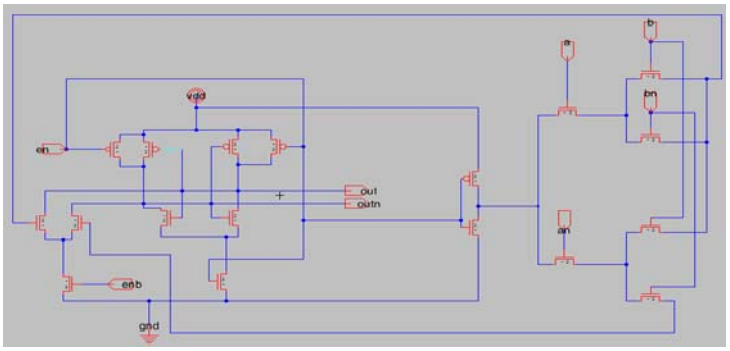


Fig 14 Schematic of pre-amplifier based clocked comparator based PTL

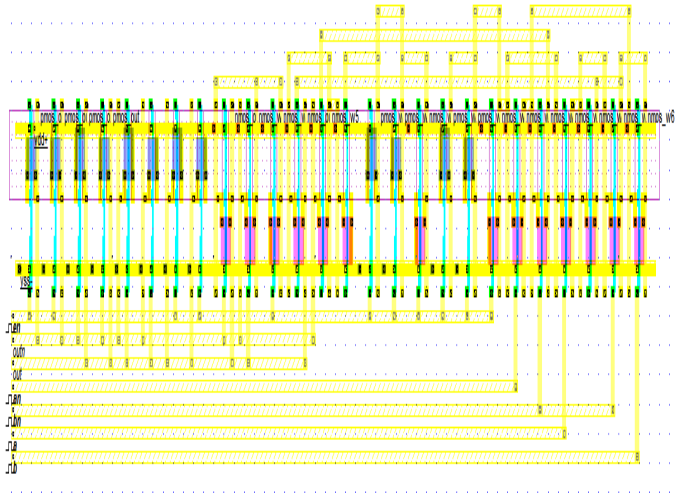


Fig 15 Layout ofpre-amplifier based clocked comparator based PTL

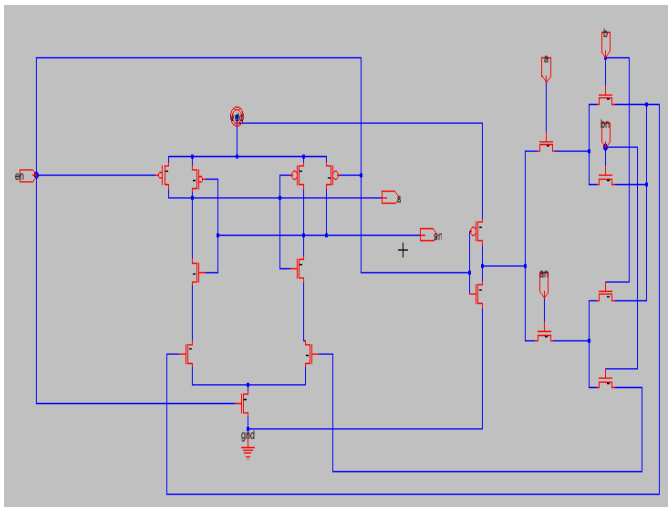


Fig 16 Schematic of dynamic latched comparator based PTL

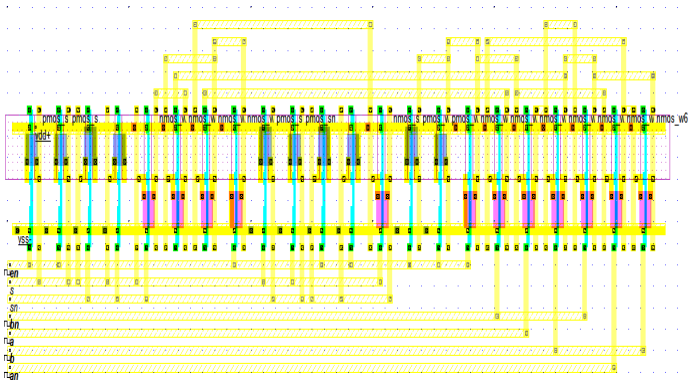


Fig 17 Layout of dynamic latched comparator based PTL

TABLE III

Comparing PTL circuit based on 3 comparators

Clocked Comparator	Transistor count	Voltage(v)	Power(mw)	Delay(ns)
Double tail Latched comparator based PTL	20	1.2	0.140	1.048
Preamplifier based clocked comparator based PTL	18	1.2	0.178	0.013
Dynamic latched comparator based PTL	17	1.2	0.006	0.011

V. SIMULATION RESULTS

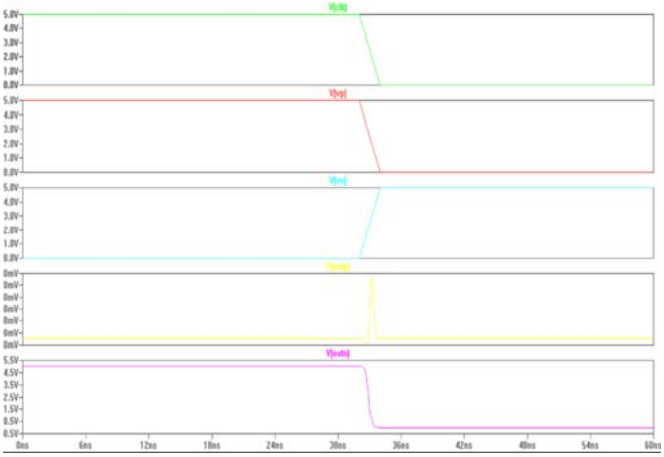


Fig 18 Waveforms of double tail latched comparator

In fig 18 double tail latched comparator compares 2 inputs, when inputs ‘vp’ > ‘vn’, then output will be ‘outn’ > ‘outp’ (‘clk’=’1’).

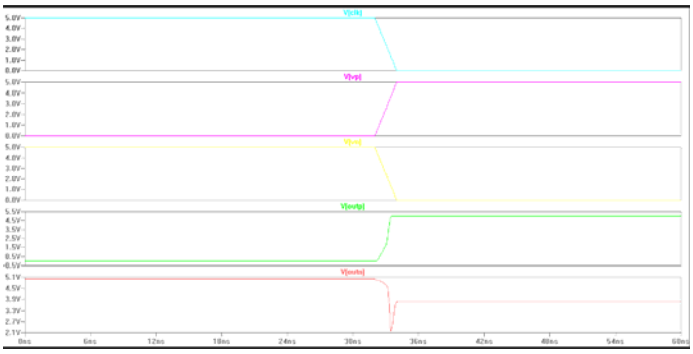


Fig 19 Waveforms of pre-amplifier based clocked comparator

In fig 19 pre-amplifier based clocked comparator compares 2 inputs, when inputs 'vp' < 'vn', then output will be 'outp' < 'outn' ('clk'='1').

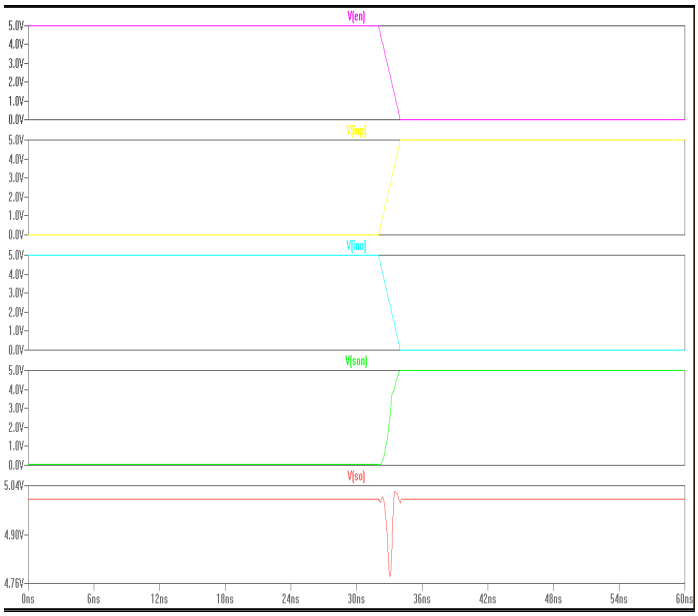


Fig 20 Waveforms of dynamic latched comparator

In fig 20 dynamic latched comparator compares 2 inputs, when inputs 'inp' < 'inn', then output will be 'son' < 'so' ('en'='1').

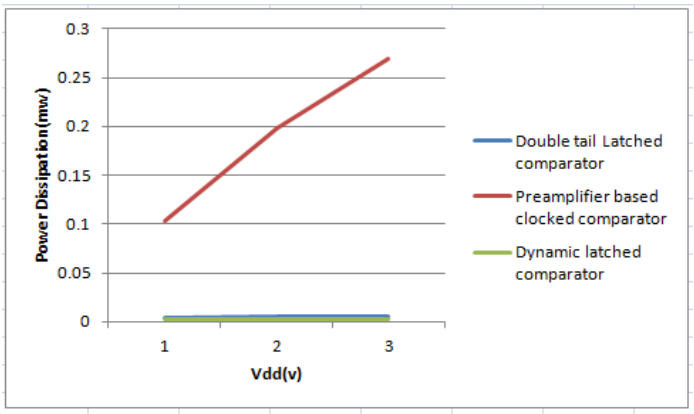


Fig 21 Comparison of Power Dissipation of the three clocked comparators

Fig 21 shows that preamplifier based comparator has more power dissipation than double tail latched comparator because of static power consumption .Dynamic latched comparator has less power consumption than the 2 conventional comparators.

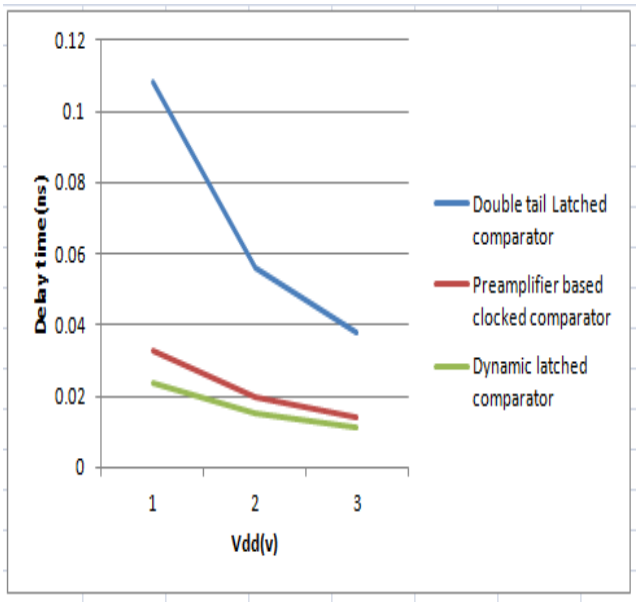


Fig 22 Comparison of delay time of the three comparators

Fig 22 shows that dynamic latched comparator has less delay time than the other two conventional comparators.

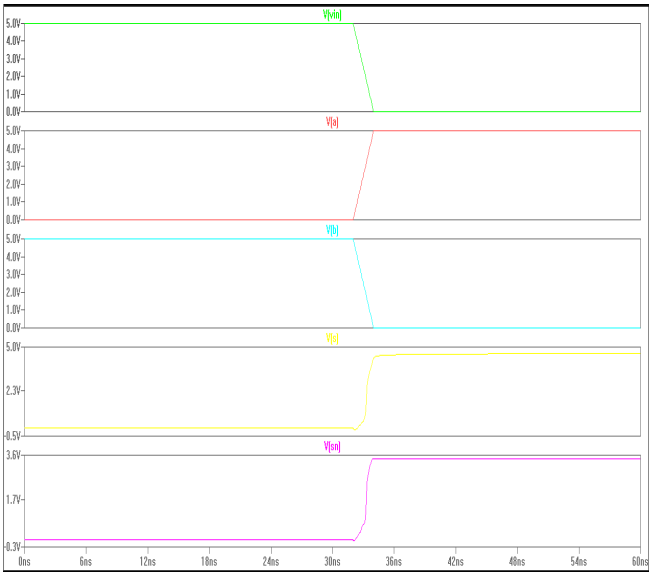


Fig 23 Waveforms of stack ckt

In Fig 23 as 'v_{in}' is '1', because of root driver (inverter), 'vin' will be provided as '0' for the stack circuit such that the stack circuit acts as NOR circuit. When 'a' is '0'and 'b' is '1', output 's' will be '0'(as input '01' is minterm only minterms output ('s') must be considered).

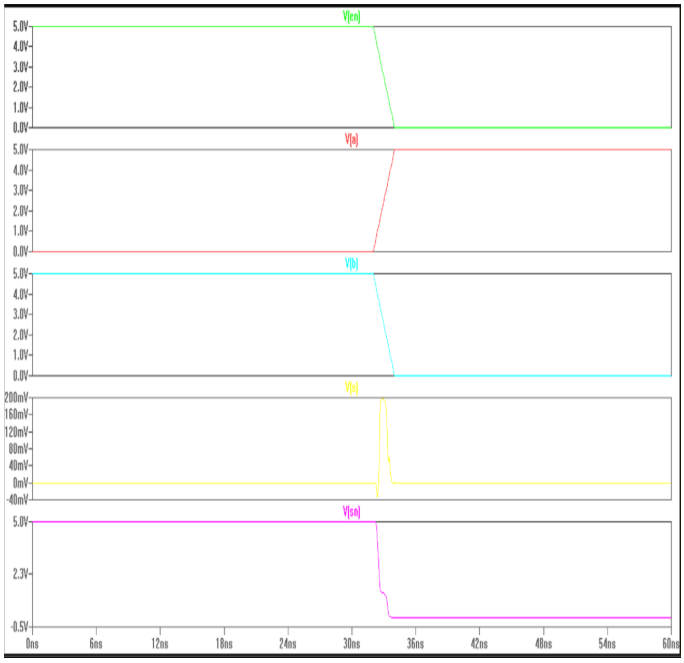


Fig 24 Waveforms of Double tail latched comparator based PTL

In fig 24, as ‘en’ is ‘1’ because of root driver (inverter), ‘en’ will be provided as ‘0’ for the stack circuit. So the stack circuit acts as NOR circuit. When ‘a’ is ‘0’and ‘b’ is ‘1’, output of double tail latched comparator based PTL will be ‘s’=‘0’(as input ‘01’ is minterm only minterms output (‘s’) of stack circuit must be considered).Therefore double tail latched comparator based PTL also performs NOR operation same as that of stack circuit.

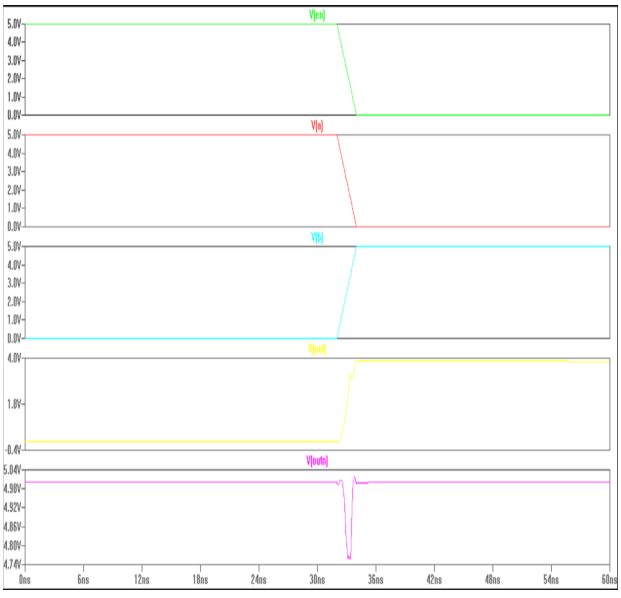


Fig 25 Waveforms of pre-amplifier based clocked comparator based PTL

In fig 25, as ‘en’ was ‘1’ because of root driver (inverter), ‘en’ will be provided as ‘0’ for the stack circuit, such that the stack circuit acts as NOR circuit. When ‘a’ is ‘1’and ‘b’ is ‘0’, output of preamplifier based comparator based PTL will be ‘out’=‘0’(as input ‘10’ is minterm only minterms output of stack circuit must be considered).Therefore double tail latched comparator based PTL also performs NOR operation same as that of stack circuit.

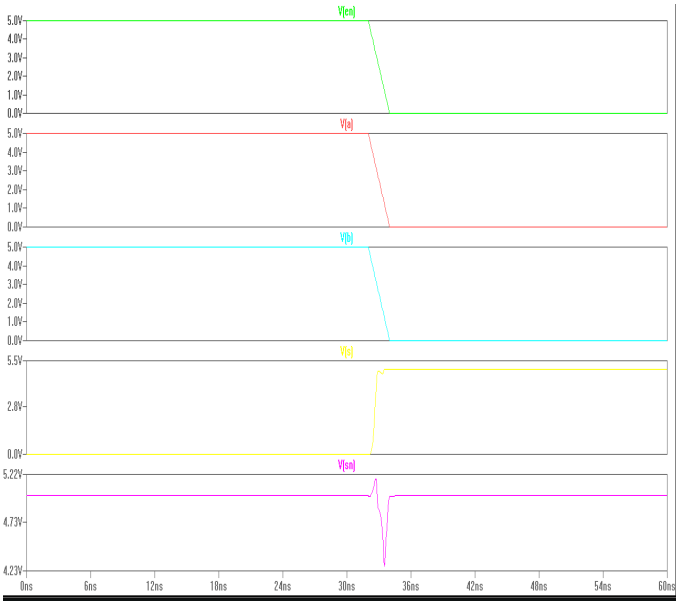


Fig 26 Waveforms of dynamic latched comparator based PTL

In fig 26 dynamic latched comparator based PTL performs NOR operation same as that of stack circuit, when ‘en’ was ‘1’ and both inputs ‘a’ , ‘b’ are 1’s output ‘s’ will be ‘0’.

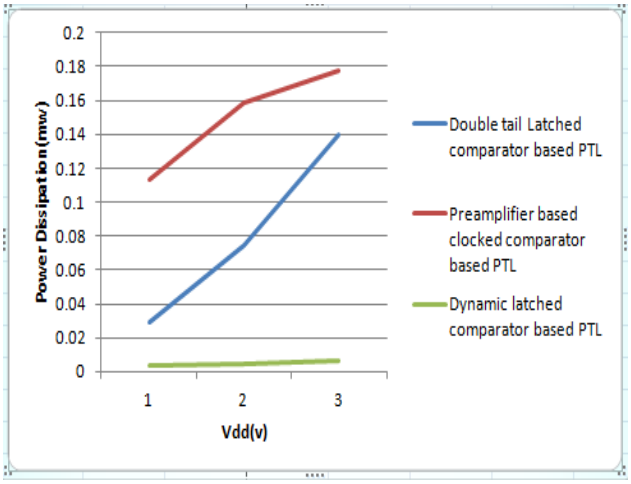


Fig 27 Comparison of power dissipation of the three comparators based PTL

Fig 27 shows that preamplifier based comparator based PTL has more power dissipation than double tail latched comparator based PTL because of static power consumption.

Dynamic latched comparator based PTL has less power consumption than the 2 conventional comparators.

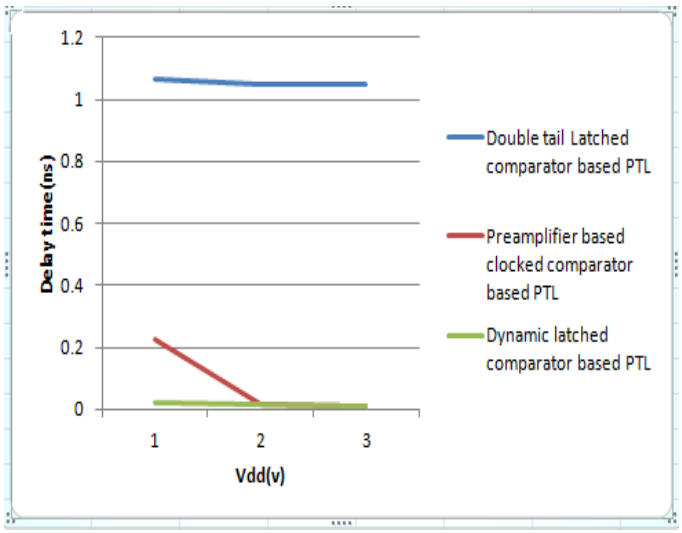


Fig 28 Comparison of delay time of the three comparators based PTL

Fig 28 shows that dynamic latched comparator based PTL has less delay time than the 2 conventional comparators based PTL

VI. CONCLUSIONS

Dynamic latched comparator was designed that works with high speed and low power consumption when compared to double tail latched comparator (conventional comparator 1) and pre amplifier based latch comparator (conventional comparator 2). For comparison we provide analog input to the comparator and the output will be digital. The simulation results show that the proposed circuit can operate at higher speed with low power dissipation than the other two comparators. Similarly in case of clocked comparator applications such as clocked comparators based PTL, dynamic latched comparator based PTL has less delay time than the other two conventional comparators based PTL. Clocked comparator schematics are implemented in spice and the corresponding layouts are implemented using microwind tool.

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